



Paolo PRINETTO

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Corso Duca degli Abruzzi, 24, Politecnico di Torino - Dip. di Automatica e Informatica,
10129, Torino, TO, Italy
Piazza S. Francesco, 19, IMT - School for Advanced Studies Lucca, 55100, Lucca, LU, Italy

AFFILIATION

CURRENT

Politecnico di Torino & IMT - School for Advanced Studies Lucca

2018 - CURRENT

Director of the CINI Cybersecurity National Laboratory

WORK EXPERIENCE

01/12/2021 - CURRENT - Turin, Italy

FULL PROFESSOR OF COMPUTER ENGINEERING (SETTORE CONCORSUALE 09/H1 - SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI, SSD ING-INF/05) - POLITECNICO DI TORINO

50% FTE

01/12/2021 - CURRENT - Lucca, LU, Italy

FULL PROFESSOR OF COMPUTER ENGINEERING (SETTORE CONCORSUALE 09/H1 - SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI, SSD ING-INF/05) - IMT - SCHOOL FOR ADVANCED STUDIES LUCCA

50% FTE

01/11/1990 - 30/11/2021 - Turin, Italy

FULL PROFESSOR OF COMPUTER ENGINEERING AT THE DIP. DI AUTOMATICA E INFORMATICA (CE DEPT) (SETTORE CONCORSUALE 09/H1 - SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI, SSD ING-INF/05) - POLITECNICO DI TORINO

2004 - 2020 - Chicago, United States

ADJUNCT PROFESSOR - UNIVERSITY OF ILLINOIS AT CHICAGO, IL (USA)

14/10/1987 - 31/10/1990 - Udine, Italy

FULL PROFESSOR OF COMPUTER SCIENCE AT THE DIP. DI STORIA (HISTORY DEPT) (GRUPPO CONCORSUALE 311: PRIMA DISCIPLINA "AUTOMI E LINGUAGGI FORMALI" - CORSO DI LAUREA IN "CONSERVAZIONE DEI BENI CULTURALI" DELLA FAC - UNIVERSITÀ DI UDINE

01/03/1982 - 13/10/1987 - Turin, Italy

01/03/1978 - 28/02/1982 - Turin, Italy

RESEARCH ASSISTANT (ASSISTENTE INCARICATO SUPPLENTE) AT THE ISTITUTO DI ELETTROTECNICA GENERALE (EE INSTITUTE) - POLITECNICO DI TORINO

EDUCATION AND TRAINING

25/10/1976 - Turin, TO, Italy

LAUREA (M.S. EQUIVALENT) IN ELECTRONIC ENGINEERING (110/110 CUM LAUDE) - Politecnico di Torino

1970 - Turin, TO, Italy

MATURITÀ SCIENTIFICA (60/60 CUM LAUDE) - Liceo Scientifico G. Segré

LANGUAGE SKILLS

Mother tongue(s): **PIEMONTEIS** | **ITALIAN**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	C2	C2	C2	C2	C2
FRENCH	C2	C2	C2	C2	C2
RUSSIAN	A1	A1	A1	A1	A1

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

TEACHING ACTIVITIES

CURRENT

Instructor of courses

[Politecnico di Torino](#) (Italy):

- 01UDNOV - Cybersecurity for Embedded Systems
- 01USBMC - Cybersecurity and National Defence

[IMT](#), Lucca (Italy):

- Introduction to Cybersecurity
- Cybersecurity and National Defence

RESEARCH ACTIVITIES

Research activities

Mainly focused on:

- *Hardware Security, Hardware-based Security, & Hardware Trust*
- *Digital Systems Design & Test*
- *Design-for-Testability, Built-in Self-Test & Built-in Self-Repair methodologies*
- *System Dependability*
- *ICT and Assistive Technologies for people with disabilities.*

RESEARCH PROJECT LEADERSHIP

Responsible of several research contracts with domestic and international Industries and Research Institutions

Including:

UE - ASI (Agenzia Spaziale Italiana) - CNR (Italian National Research Council) - [Ministero dell'Istruzione, dell'Università e della Ricerca](#) - Istituto Superiore Mario Boella - EDF Electricité De France (France) - ASSET (USA) - Siemens ICN - Italtel SpA - Ansaldo Trasporti - Ansaldo Signalling - ThalesAlenia Space - Magneti Marelli - Bottero - Selca - Aurelia Microelettronica - Yogitech - Blu5 (Malta) - MBDA.

CONFERENCES AND SEMINARS

Conference Board Membership

Chair of the Steering Committees of the following international conference:

2014-2016

IEEE ETS: European Test Symposium (2014 - 2016)

2018-2019

ITASEC: Italian Conference on Cybersecurity (2018 - 2019)

Conference Board Membership

General Chair of the following international conferences and workshops:

2022

- ITASEC22: Italian Conference on Cybersecurity, Rome (June 2022) (General Co-Chair)

2021

- EWDTs 2021: East West Design and Test Symposium, Batumi (Georgia) (September 2021) (Vice General Chair)
- ITASEC21: Italian Conference on Cybersecurity, on-line (April 2021) (General Co-Chair)

2020

- EuroS&P 2020: IEEE European Symposium on Security and Privacy 2020 on-line (September 2020) (General Co-Chair)
- EWDTs 2020: East West Design and Test Symposium, Varna (Bulgaria) (September 2020) (Vice General Chair)
- ITASEC20: Italian Conference on Cybersecurity, Ancona (Italy) (February 2020) (General Co-Chair)

HONOURS AND AWARDS

29/11/2010

Doctor Honoris Causa – Technical University of Cluj-Napoca (Romania)

"Pentru contributia remarcabila in domeniul proiectarii si testarii sistemelor digitale si pentru activitatea de exceptie in statornicirea si dezvoltarea relatiilor de colaborare dintre universitatile noastre"

2015, 2005, 2004, 2000, 1999 & 1993

27/12/2019

Onorificenza di Cavaliere – Il Presidente della Repubblica

"In considerazione di particolari benemerienze, su proposta del Presidente del Consiglio dei Ministri"
Registrato nell'albo dei Cavalieri al N. 13025 Serie VI

● **PROFESSIONAL INVOLVEMENTS**

International

2021-Today

Appointed by the Italian *Ministry of University and Research*, as Italian Representative in the *Programme Committee for the specific programme implementing Horizon Europe - the Framework Programme for Research and Innovation – Civil Security for Society*

2020-2021

Appointed by the Italian *Ministry of Education, University and Research*, as Italian Representative in the *Civil Security for Society* sub-group of the *EU Shadow Strategic Programme Committee*

2010-2014

Member of the Scientific Committee of the *Centre National de la Recherche Scientifique (C.N.R.S.)* (the French National Research Council), a government-funded research organization, under the administrative authority of France's Ministry of Research - (<http://www.cnrs.fr/comitenational/cs/membres.htm>)

2010-2016

Member of the Scientific Committee of the *International Test Spring School* organized yearly by the IEEE ETS Steering Committee

2013-2018

Vice-Chair of the IFIP (International Federation for Information Processing) Technical Committee TC 10 - Computer Systems Technology aimed at "promoting the State-of-the-Art and the coordination of information exchange on concepts, methodologies, and tools in the stages in the life cycle of computer systems"

2000-2003

Chair of the IEEE - Computer Society TTTC: Test Technology Technical Council. The TTTC is a worldwide professional organization sponsored by the IEEE Computer Society. TTTC's goals are to contribute to members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art.

Domestic

2018-today

Director of the CINI Cybersecurity National Laboratory <https://cybersecnatlab.it>

2021-today

Coordinator of the program *OliCyber.IT*: the Italian Cybersecurity Olympiad: the first cybersecurity training and competition program entirely devoted to high school students - <https://olicyber.it>

2019-today

Coordinator of the program *CyberChallenge.IT*: the main Italian initiative aiming at identifying, attracting, recruiting, and placing the next generation of IT security professionals - <https://cyberchallenge.it>

2013-2018

President of CINI (Consorzio Interuniversitario Nazionale per l'Informatica): a consortium of 47 Italian universities that do research in Computer Engineering & Computer Science, deliver MS/PhD degrees, and are public funded) - <http://www.consorzio-cini.it>

● PUBLICATIONS

CFI: Control Flow Integrity or Control Flow Interruption?

2019
IEEE East-West Design & Test Symposium (EWDTS), pp. 1-6
Authors: Maunero, Nicolò; Prinetto, Paolo; Roascio, Gianluca

Il Futuro della Cybersecurity in Italia: Ambiti Progettuali Strategici - Progetti e Azioni per difendere al meglio il Paese dagli attacchi informatici

CINI - Cybersecurity National Laboratory
<https://cybersecnatlab.it/projects/white-book/?lang=en> – 2018
Authors: Baldoni, Roberto; De Nicola, Rocco; Prinetto, Paolo

English Version: The Future of Cybersecurity in Italy: Strategic Project Areas - *Projects and Actions to better defend the Country from cyber attacks*

Scan chain encryption for the test, diagnosis and debug of secure circuits

2017
22nd IEEE European Test Symposium (ETS), pp. 1-6
Authors: Da Silva, Mathieu; Flottes, Marie Lise; Di Natale, Giorgio; Rouzeyre, Bruno; Prinetto, Paolo; Restifo, Marco

STT-MRAM-based PUF architecture exploiting magnetic tunnel junction fabrication-induced variability

2016
ACM Journal on Emerging Technologies in Computing Systems (JETC), 13, 1, 5
Authors: Vatajelu, Elena Ioana; Di Natale, Giorgio; Barbareschi, Mario; Torres, Lionel; Indaco, Marco; Prinetto Paolo

SSDEXplorer: a Virtual Platform for Performance/Reliability-oriented Fine-Grained Design Space Exploration of Solid State Drives

2015
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 34, 10, 1627-1638
Authors: Zuolo, Lorenzo; Zambelli, Cristian; Micheloni, Rino; Indaco, Marco; Di Carlo, Stefano; Prinetto, Paolo; Bertozzi, Davide; Olivo, Piero

Lists of Prof. Paolo Prinetto's most significant international publications can be found at:

www.scholar.google.com - <http://scholar.google.com/citations?user=KK2B5igAAAAJ>
www.scopus.com - <http://www.scopus.com/authid/detail.url?authorId=7005222576>

According to law 679/2016 of the Regulation of the European Parliament of 27th April 2016, I hereby express my consent to process and use my data provided in this CV

Turin, 07/05/2022



Paolo PRINETTO